JL7012A Datasheet

Zhuhai Jieli Technology Co.,LTD

Version：2.1

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JL7012A Features

CPU

- 32bit Dual-Core DSP
- Maximum speed 160MHz
- 32KB ICache and 16KB DCache
- IEEE754 Single precision FPU
- Mathematical accelerate engine
- Interrupts with 8 priority level

Memory

- On-chip 640KB SRAM
- Support MMU
- Built-In Flash
- SPI PSRAM controller

Clocks

- On-chip 16 MHz clock oscillator
- On-chip 200 kHz lower-temperature-drift clock oscillator
- 24 MHz crystal oscillator
- 32.768 kHz crystal oscillator

DSP Audio Processing

- LDAC, LHDC, SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Single/Dual MIC Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- Multi-band EQ configuration for voice Effects
- Support Hi-Res Audio

Audio Codec

- Two channels 24-bit DAC,SNR ≥ 98dB
- Four channels 24-bit ADC,SNR ≥ 95dB
- Audio DAC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/ 32kHz/44.1kHz/48kHz/64kHz/88.2kHz/ 96kHz are supported
- Audio ADC Sampling rates of 8kHz/11.025kHz/16kHz/22.05kHz/24kHz/32 kHz/44.1kHz/48kHz are supported
- Support four digital/analog MIC inputs
- Four channels analog audio inputs
- Audio DAC support differential cap-less mode or single-ended mode
- Direct drive 16ohm/32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth V6.0+BR+EDR+BLE specification (DN Q332415)
- Support AoA/AoD direction finding
- Support LE audio BIS/CIS full function
- Meet class1,class2 and class3 transmitting power requirement
- Maximum +9dbm transmitting power
- EDR receiver with minimum -95dBm sensitivity
- Support a2dp\avctp\avdtp\avrcp\hfp\spp\smp\ att\gap\gatt\rfcomm\sdp\l2cap profile
- bap 1.0.2\pacs 1.0.2\ccp 1.0\mcp 1.0\micp 1.0\vcp 1.0\csip1.0.1\ascs1.1\bass1.0\cap 1.0\hap 1.0\pbp 1.0.1\tmap 1.0\lc3 1.0.1
- a2dp 1.4\avctp 1.4\avdtp 1.3\ avrcp 1.6.3\ hfp 1.9\spp 1.2\rfcomm 1.2\pnp 1.3\ hid 1.1.1\sdp core 6.0\l2cap core 6.0

Graphics

- 2D Graphics accelerator
- Support crop, scale, rotation process
- Support multiple data format graphics
- SPI and QSPI display driver

Peripherals

- One full speed USB OTG controller
- One SD host controller for eMMC/SD

- Six multi-function 32-bit timers, support capture and PWM mode
- Four UART interface, UART0,UART1&UART2 support DMA
- Two I2C Master/Slave interface
- Four SPI Master/Slave interface
- I2S master/slave interface supports sampling rates from 8kHz to 192kH
- PDM slave interface supports sampling rates from 8kHz to 192kHz
- QDEC
- Low power CapSense
- 15-channel 10-bit ADC for analog sampling
- 4-channel Motor PWM controller
- 40 Individually programmable and multiplexed GPIO pins
- Up to 12 external interrupt/wake-up source(low power available,can be multiplexed to any I/O)

PMU

- Built-in lithium battery charging manager,up to 200mA charging current
- Built-in LDO and Buck DC-DC converter
- Less than 2uA sleep current
- RTC sleep current is 8uA
- VPWR range : 4.5V to 5.5V
- VBAT range : 2.2V to 4.5V
- IOVDD range : 2.2V to 3.6V
- Conform with IEC 62368-1:2018 certification

Packages

- QFN52(6mm*6mm)

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Applications

- Bluetooth Smart Watch
- Bluetooth Smart Home
- Bluetooth Intelligent Voice
- Bluetooth Stereo speaker
- Bluetooth TWS speaker
- Bluetooth alarm clock speaker

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1 Block Diagram

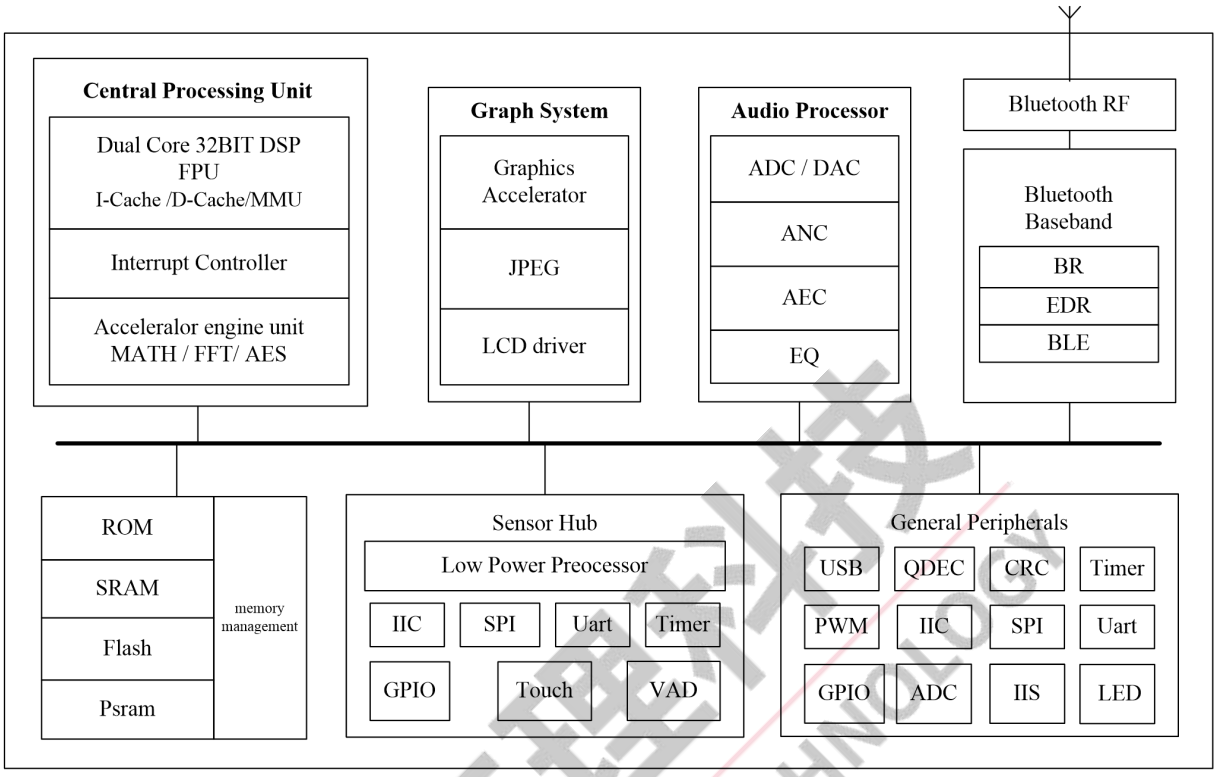


Figure 1-1 JL7012A Block Diagram

2 Pin Definition

2.1 Pin Assignment

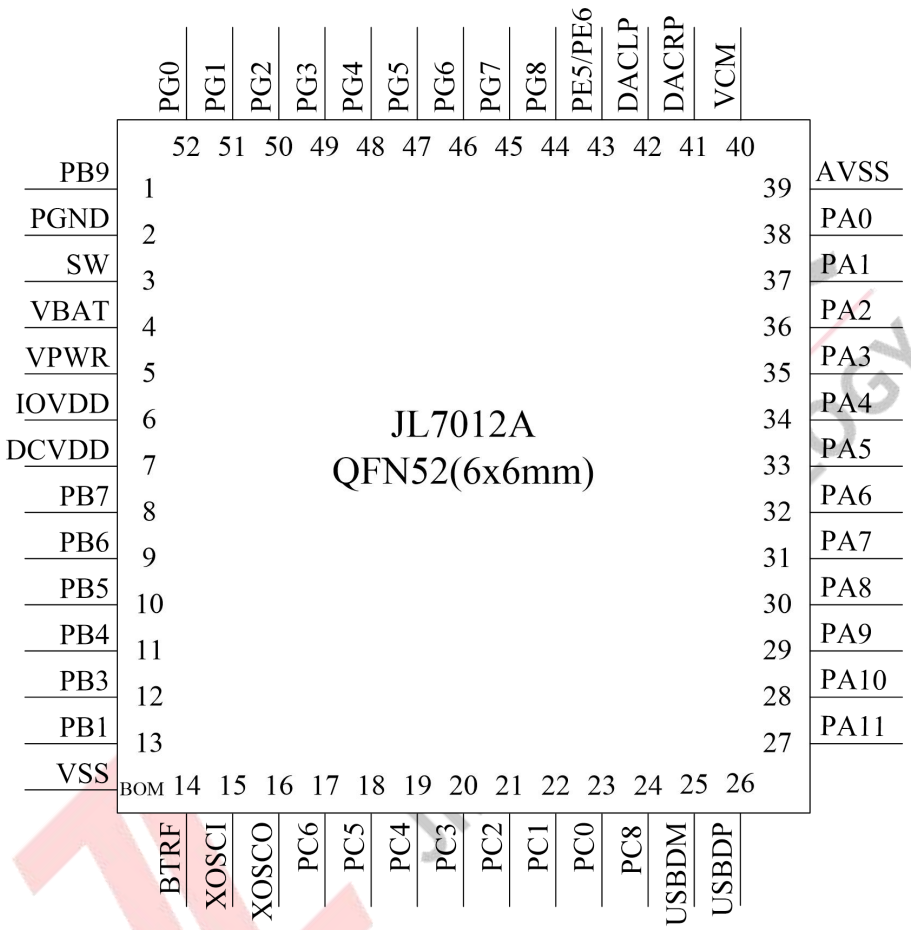


Figure 2-1 JL7012A Package Diagram

2.2 Pin Description

Table 2-1 JL7012A Pin Description

PIN NO.	Name	Type	Function	Other Function
1	PB9	I/O	GPIO	ADC9:ADC Input Channel 9;
2	PGND	G		The ground of Buck DC-DC converter;
3	SW	PO		Switch signal of the Buck converter,Connected to inductor;
4	VBAT	P		Battery interface;
5	VPWR (PP0)	PI (I/O)	GPIO	Charging power input; UART0TXB:Uart0 Data Output(B); UART0RXB:Uart0 Data Input(B); CAP1:Timer1 Capture; PWM3:Timer3 PWM Output;
6	IOVDD	PO		Built-in linear voltage regulator output;
7	DCVDD	P		Internal power;
8	PB7	I/O	GPIO	OSC32KI:32.768khz crystal oscillator input;
9	PB6	I/O	GPIO	OSC32KO:32.768khz crystal oscillator output; PWM2:Timer2 PWM Output;
10	PB5	I/O	GPIO	LP_Touch4:Low Power Touch Channel 4; IIC1_SDA_A:IIC1 SDA(A); ADC8:ADC Input Channel 8; UART3RXB:Uart3 Data Input(B);
11	PB4	I/O	GPIO	LP_Touch3:Low Power Touch Channel 3; CLKOUT0:Clock Out0; IIC1_SCL_A:IIC1 SCL(A); UART3TXB:Uart3 Data Output(B); TMR2:Timer2 Clock Input;
12	PB3	I/O	GPIO	UART3RXA:Uart3 Data Input(A);
13	PB1	I/O	GPIO (pull up)	Hold down 0 to reset; LP_Touch1:Low Power Touch Channel 1; ADC6:ADC Input Channel 6;
14	BTRF	RFI		Bluetooth RF antenna interface;
15	XOSCI	I		System Crystal Oscillator Input;
16	XOSCO	O		System Crystal Oscillator Output;
17	PC6	I/O	GPIO (High Voltage Resistant)	ALNK_MCLKB:ALNK Master Clock(B);

18	PC5	I/O	GPIO	SFC1_D2:SFC1 Data2(nor flash); SPI0_DAT2C(2):SPI0 Data2(C); SD0_CLKA:SD0 Clock(A); SPI1DOB:SPI1 Data Out(B); IIC0_SDA_B:IIC0 SDA(B); ALNK_DAT3(B):Audio Link Data3(B); ADC5:ADC Input Channel 5; UART2RXA:Uart2 Data Input(A);
19	PC4	I/O	GPIO	SFC1_DI(D1):SFC1 Data In(nor flash); SPI0_DIC(1):SPI0 Data In(C); SD0_CMDA:SD0 CMD(A); SPI1CLKB:SPI1 Clock(B); IIC0_SCL_B:IIC0 SCL(B); ALNK_DAT2(B):Audio Link Data2(B); ADC4:ADC Input Channel 4; UART2TXA:Uart2 Data Output(A); PWM4:Timer4 PWM Output;
20	PC3	I/O	GPIO	SFC1_CS:SFC1 Chip Select(nor flash); LNA_EN:LNA Enable; SPI0_CSC:SPI0 Chip Select(C); SD0_DATA:SD0 Data(A); SPI1DIB:SPI1 Data In(B); ALNK_LRCK(B):Audio Link Word Select(B); TMR3:Timer3 Clock Input;
21	PC2	I/O	GPIO	SFC1_DO(D0):SFC1 Data Out(nor flash); PA_EN:PA Enable; SPI0_DOC(0):SPI0 Data Out(C); ALNK_SCLK(B):Audio Link Serial Clock(B); TMR1:Timer1 Clock Input;
22	PC1	I/O	GPIO	SFC1_CLK:SFC1 Clock(nor flash); SPI0_CLKC:SPI0 Clock(C); ALNK_DAT1(B):Audio Link Data1(B); TMR5:Timer5 Clock Input; PWMCH1L:Motor PWM Channel1(L);
23	PC0	I/O	GPIO	SFC1_D3:SFC1 Data3(nor flash); SPI0_DAT3C(3):SPI0 Data3(C); ALNK_DAT0(B):Audio Link Data0(B); PWMCH1H:Motor PWM Channel1(H);
24	PC8	I/O	GPIO	SPI2DIB:SPI2 Data In(B);
25	USBDM	I/O	USB Negative Data (pull down)	SPI2DOB:SPI2 Data Out(B); IIC0_SDA_A:IIC0 SDA(A); ADC11:ADC Input Channel 11; UART1RXB:Uart1 Data Input(B);

26	USBDP	I/O	USB Positive Data (pull down)	SPI2CLKB:SPI2 Clock(B); IIC0_SCL_A:IIC0 SCL(A); ADC10:ADC Input Channel 10; UART1TXB:Uart1 Data Output(B);
27	PA11	I/O	GPIO	LCD_SPID3(A); FPIN0;
28	PA10	I/O	GPIO	LCD_SPID2(A); FPIN3;
29	PA9	I/O	GPIO	LCD_SPID1(DI)(A); PWMCH0H:Motor PWM Channel0(H);
30	PA8	I/O	GPIO	LCD_SPID0/DO(A); PLNK_DAT1/ANCDE; ALNK_LRCK(A):Audio Link Word Select(A); ADC3:ADC Input Channel 3; UART2RXB:Uart2 Data Input(B);
31	PA7	I/O	GPIO	LCD_SPICLK(A); ALNK_SCLK(A):Audio Link Serial Clock(A); UART2TXB:Uart2 Data Output(B); TMR0:Timer0 Clock Input;
32	PA6	I/O	GPIO	PLNK_DAT0/ANCDR; SPI2DOA:SPI2 Data Out(A); ALNK_DAT3(A):Audio Link Data3(A); ADC2:ADC Input Channel 2; UART0RXA:Uart0 Data Input(A); CAP0:Timer0 Capture;
33	PA5	I/O	GPIO	PLNK_SCLK/ANCCK; SPI2CLKA:SPI2 Clock(A); ALNK_DAT2(A):Audio Link Data2(A); ADC1:ADC Input Channel 1; UART0TXA:Uart0 Data Output(A); PWM5:Timer5 PWM Output;
34	PA4	I/O	GPIO	MIC_BIAS1:MIC1 Bias Output(Built-in resistor); MIC1_N:Different MIC1 Negative; AMUX_B1:Analog Channel B1 input; SPI2DIA:SPI2 Data In(A); ALNK_DAT1(A):Audio Link Data1(A); CAP2:Timer2 Capture;
35	PA3	I/O	GPIO	MICIN1:MIC1 Input Channel 1; MIC1_P:Different MIC1 Positive; AMUX_B0:Analog Channel B0 input; SPI1DOA:SPI1 Data Out(A); ALNK_DAT0(A):Audio Link Data0(A); PWM1:Timer1 PWM Output;

36	PA2	I/O	GPIO	MIC_BIAS0:MIC0 Bias Output(Built-in resistor); MIC0_N:Different MIC0 Negative; AMUX_A1:Analog Channel A1 input； CLKOUT1:Clock Out1; SPI1CLKA:SPI1 Clock(A); ALNK_MCLKA:ALNK Master Clock(A); UART1RXA:Uart1 Data Input(A); CAP3:Timer3 Capture;
37	PA1	I/O	GPIO	MICIN0:MIC0 Input Channel 0; MIC0_P:Different MIC0 Positive; AMUX_A0:Analog Channel A0 input； SPI1DIA:SPI1 Data In(A); UART1TXA:Uart1 Data Output(A); PWM0:Timer0 PWM Output;
38	PA0	I/O	GPIO	MICLDO:Microphone linear voltage regulator output; ADC0:ADC Input Channel 0;
39	AVSS	G		Audio analog ground;
40	VCM	P		Audio analog reference bias;
41	DACRP	AO		Right channel audio output positive;
42	DACLP	AO		Left channel audio output positive;
43	PE6	I/O	GPIO	SDPG:SD card power gate;
	PE5	I/O	GPIO	
44	PG8	I/O	GPIO	MICIN2:MIC2 Input Channel 2; MIC2_P:Different MIC2 Positive; AMUX_C0:Analog Channel C0 input；
45	PG7	I/O	GPIO	LCD_SPID3(B); MIC_BIAS2:MIC2 Bias Output(Built-in resistor); MIC2_N:Different MIC2 Negative; AMUX_C1:Analog Channel C1 input； ADC15:ADC Input Channel 15;
46	PG6	I/O	GPIO	LCD_SPID2(B); MICIN3:MIC3 Input Channel 3; MIC3_P:Different MIC3 Positive; AMUX_D0:Analog Channel D0 input； FPIN2;
47	PG5	I/O	GPIO	LCD_SPID1/DI(B); MIC_BIAS3:MIC3 Bias Output(Built-in resistor); MIC3_N:Different MIC3 Negative; AMUX_D1:Analog Channel D1 input； ADC14:ADC Input Channel 14; TMR3CK;
48	PG4	I/O	GPIO	LCD_SPID0/DO(B); PWMCH3L:Motor PWM Channel3(L);

49	PG3	I/O	GPIO	LCD_SPICLK(B); TDM_MCLK; PWMCH3H:Motor PWM Channel3(H);
50	PG2	I/O	GPIO	TDM_DAT; SD0_CLKB:SD0 Clock(B); PWMCH2L:Motor PWM Channel2(L);
51	PG1	I/O	GPIO	TDM_SYN; SD0_CMDB:SD0 CMD(B); ADC13:ADC Input Channel 13; PWMCH2H:Motor PWM Channel2(H);
52	PG0	I/O	GPIO	TDM_CLK; LVD:Low Voltage Detect; SD0_DATB:SD0 Data(B); ADC12:ADC Input Channel 12; TMR2CK;
BOM	VSS	G		System ground;

Pin Type	**Description**	**Pin Type**	**Description**
P	Power	I/O	Input or Output
PO	Power Output	I	Input
PI	Power Input	O	Output
G	Ground	RFI	Radio frequency interface
AO	Analog Output		

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	4.5	V
VPWR	Charger Voltage	-0.3	6	V
V_{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V_{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
V_{HVIO}	Voltage applied to High Voltage Resistant IO	-0.3	Minimum between IOVDD*2 and +5.0V	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

3.2 PMU Characteristics

Table 3-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	4.5	V	
VPWR	Charger supply Voltage	4.5	5.0	5.5	V	
Operating mode						
IOVDD	Voltage output	2.0	3.0	3.4	V	VBAT = 4.2V, 10mA loading
	Loading current	_	_	120	mA	IOVDD=3V@VBAT = 4.2V
DCVDD	Voltage output	1.0	1.25	1.4	V	IOVDD=3.0V, 10mA loading
	Loading current	_	_	100	mA	DCVDD=1.25V@IOVDD=3.0v On LDO mode
		_	_	180	mA	DCVDD=1.25V@IOVDD=3.0v On DC-DC mode
V_{LVD}	Voltage input	1.8	2.5	2.5	V	Low-Voltage Detection for IOVDD
Low Power mode						
IOVDD	Loading current	_	_	10	mA	IOVDD=3V@VBAT = 4.2V

3.3 Battery Charge

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{PWR}	Charge Input Voltage Range	4.5	5	5.5	V	_
$V_{BAT\ Float}$	Battery Charge Termination Voltage	4.15	4.2	4.25	V	VPWR＞4.5V
		4.30	4.35	4.40	V	VPWR＞4.65V
I_{BAT}	Fast Charge Current	15	_	200	mA	VBAT=4.0V@VPWR=5.0V
I_{END}	Charge Termination Current Threshold	2	_	30	mA	_
V_{Trikl}	Trickle Charge Voltage	_	3.0	_	V	VPWR＞4.5V
I_{Trikl}	Trickle Charge Current	1.5	_	30	mA	V_{BAT}<V_{Trikl}

3.4 IO Input/Output Electrical Logical Characteristics

Table 3-4

GPIO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	IOVDD+0.3	V	IOVDD = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	_	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	_	+5V	V	IOVDD = 3.0V
GPIO & High Voltage Resistant IO output characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{OL}	Low-Level Output Voltage	_	_	0.1* IOVDD	V	IOVDD = 3.0V
V_{OH}	High-Level Output Voltage	0.9* IOVDD	_	_	V	IOVDD = 3.0V

3.5 Internal Resistor Characteristics

Table 3-5

Port	Drive Current		Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA0~PA11 PC0~PC5,PC8 PG0~PG8 PE5,PE6	HD1,HD0==0,1	8mA	10K	10K	1. PB1 default pull up 2. USBDM & USBDP default pull down 3. Internal pull-up/pull-down resistance | accuracy ±20%
	HD1,HD0==1,0	26mA			
	HD1,HD0==1,1	46mA			
PB1~PB9 PC6 PP0(VPWR)	8mA		10K	10K	
USBDP	4mA		1.5K	15K	
USBDM	4mA		180K	15K	

3.6 Audio DAC Characteristics

Table 3-6

Parameter	MODE	Min	Typ	Max	Unit	Test Conditions
Frequency Response		20	_	20K	Hz	1KHz/0dB 10k ohm loading With A-Weighted Filter
Output Swing	Differential	_	1	_	Vrms	
	Single-ended	_	520	_	mVrms	
THD+N	Differential	_	-70	_	dB	
	Single-ended	_	-70	_	dB	
S/N	Differential	_	104	_	dB	
	Single-ended	_	98	_	dB	
Dynamic Range	Differential	_	104	_	dB	1KHz/-60dB 10k ohm loading With A-Weighted Filter
	Single-ended	_	98	_	dB	
Noise Floor	Differential	_	5.8	_	uVrms	A-Weighted Filter
	Single-ended	_	5.8	_	uVrms	

3.7 Audio ADC Characteristics

Table 3-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range	_	94	_	dB	Fsample=44.1kHz,Gain=0dB Fin=1KHz 590mVrms
S/N	_	95	_	dB	Fsample=44.1kHz,Gain=0dB Fin=1KHz 590mVrms
THD+N	_	-75	_	dB	
S/N	_	76	_	dB	Fsample=44.1kHz,Gain=18dB Fin=1KHz 75mVrms
THD+N	_	-73	_	dB	

3.8 BT Characteristics

3.8.1 Transmitter BDR & EDR

Basic Data Rate **Table 3-8**

Parameter		Min	Typ	Max	Unit	Test Conditions
RF Transmit Power			7.0		dBm	25℃, Power Supply VBAT=3.7V 2441MHz 4 Layer Board
RF Power Control Range			18.2		dB	
20dB Bandwidth			950		KHz	
In-band spurious Emissions （BQB Test Mode RF_Tx Power=5dBm）	F=F0±1MHz		-22		dBm	
	F=F0±2MHz		-51		dBm	
	F=F0±3MHz		-55		dBm	
	F=F0+/->3MHz		-55		dBm	

Enhanced Data Rate **Table 3-9**

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-2.5		dB	25℃ Power Supply VBAT=3.7V 2441MHz 4 Layer Board
π/4 DQPSK Modulation Accuracy	DEVM RMS		6		%	
	DEVM 99%		11		%	
	DEVM Peak		16		%	
In-band spurious Emissions （BQB Test Mode RF_Tx Power=5dBm）	F=F0±1MHz		-4		dBm	
	F=F0±2MHz		-34		dBm	
	F=F0±3MHz		-43		dBm	
	F=F0+/->3MHz		-48		dBm	

3.8.2 Receiver BDR & EDR

Basic Data Rate **Table 3-10**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-92		dBm	25℃ Power Supply VBAT=3.7V 2441MHz DH5 4 Layer Board
Co-channel Interference Rejection			10		dB	
Adjacent Channel selectivity C/I	+1MHz		-4		dB	
	-1MHz		-3		dB	
	+2MHz		-39		dB	
	-2MHz		-33		dB	
	+3MHz		-45		dB	
	-3MHz		-28		dB	

Enhanced Data Rate **Table 3-11**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity		-95	-94		dBm	25℃ Power Supply VBAT=3.7V 2441MHz 2DH5 4 Layer Board
Co-channel Interference Rejection			10		dB	
Adjacent Channel selectivity C/I	+1MHz		-8		dB	
	-1MHz		-8		dB	
	+2MHz		-40		dB	
	-2MHz		-33		dB	
	+3MHz		-45		dB	
	-3MHz		-27		dB	

3.8.3 BLE

1M Data Rate **Table 3-12**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-97		dBm	25℃ Power Supply VBAT=3.7V 2441MHz 4 Layer Board
RF Transmit Power			6.5		dBm	
In-band Spurious Emission	|M-N|=2MHz			-40	dBm	
	|M-N|≥3MHz			-50	dBm	
Modulation Characteristics	Δf1 avg		250		KHz	
	Δf2 99%		200		KHz	
	Δf1avg/Δf2avg		0.9		/	
Carrier Frequency Offset		-10		+10	KHz	
Frequency Drift		-10		+10	KHz	
Frequency Drift Rate		-5		+5	KHz/50us	

2M Data Rate **Table 3-13**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-94		dBm	25℃ Power Supply VBAT=3.7V 2441MHz 4 Layer Board
RF Transmit Power			6.5		dBm	
In-band Spurious Emission	|M-N|=4MHz			-40	dBm	
	|M-N|=5MHz			-40	dBm	
	|M-N|≥6MHz			-50	dBm	
Modulation Characteristics	Δf1 avg		500		KHz	
	Δf2 99%		415		KHz	
	Δf1avg/Δf2avg		0.9		/	
Carrier Frequency Offset		-10		+10	KHz	
Frequency Drift		-10		+10	KHz	
Frequency Drift Rate		-5		+5	KHz/50us	

Long Range **Table 3-14**

Parameter	Min	Typ	Max	Unit	Test Conditions
Sensitivity LE 125K(S8)		-104		dBm	VBAT=3.7V,25℃ 2441MHz
Sensitivity LE 500K(S2)		-101		dBm	

3.9 ESD Protection

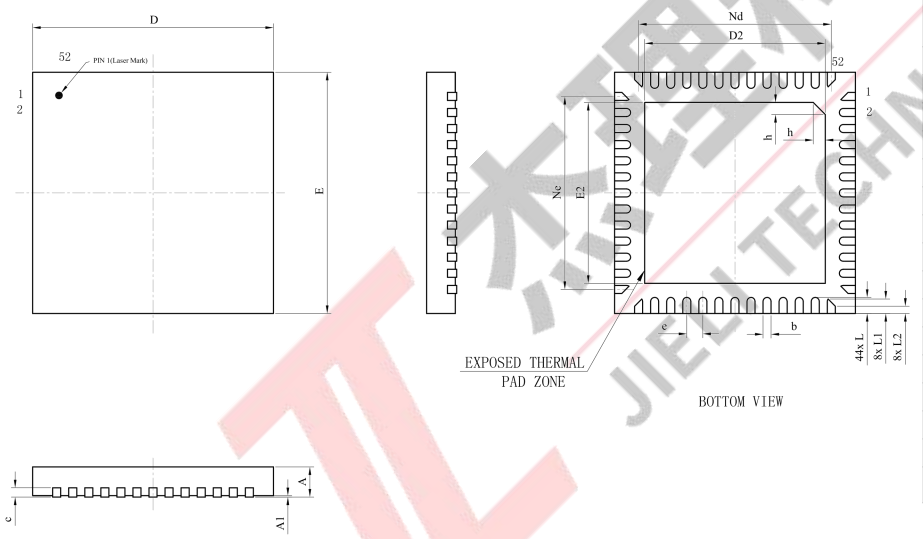
Table 3-15

Parameter	Typ.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±1KV	All pins	JEDEC EIA/JESD22-C101F
Latch up	±200mA	All GPIO pins	JEDEC STANDARD NO.78E
	1.5xVopmax	All power pins	

Note : 1.5xVopmax = 1.5 times maximum operating voltage.

4 Package Information

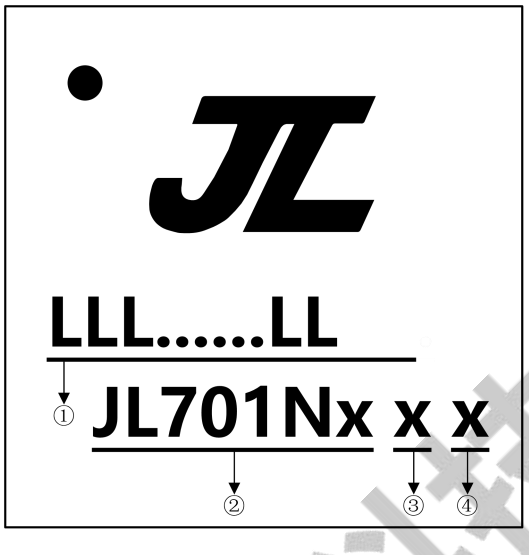
4.1 QFN52_6×6mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.65	0.80	0.95
A1	--	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40BSC		
Nd	4.80BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F 载体尺寸 (mil)	185*185		

Figure 4-1 JL7012A Package

5 IC Marking Information



① LLL.....LL：LOT No. , It contains 7 to 18 alphanumerics

② JL701Nx: Chip Model

③ x: Built-in flash size

0: No Flash Memory
2: 2Mbit Flash
4: 4Mbit Flash
8: 8Mbit Flash
6: 16Mbit Flash
3: 32Mbit Flash
5: 64Mbit Flash
7: 128Mbit Flash

④ x:Built-in Psram size

Space:No Psram Memory
S:16Mbit Psram
T:64Mbit Psram

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6 Solder-Reflow Condition

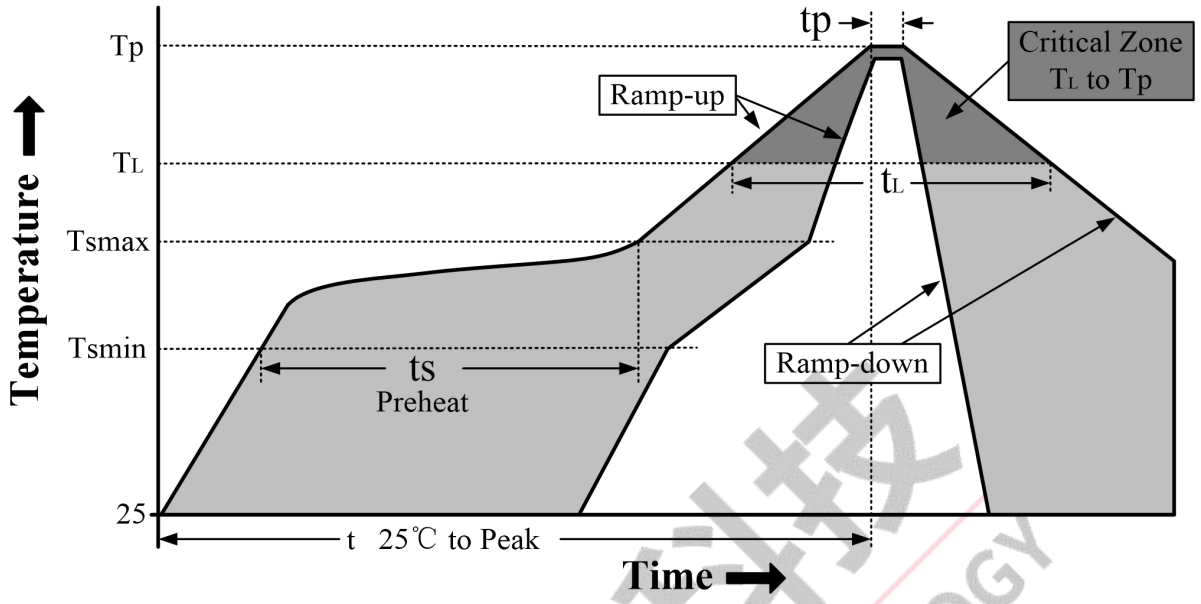


Figure 6-1 Classification Reflow Profile

Classification Profiles **Table 6-1**

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/ Soak	Temperature Min (T_{smin})	100 °C	150 °C
	Temperature Max (T_{smax})	150 °C	200 °C
	Time (ts) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3 °C/second max	3 °C/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L		183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)		See Table 6-2.	See Table 6-3.
Time within 5°C of actual Peak Temperature (tp)		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature		6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5°C of actual peak temperature (tp) specified for the reflow profiles is a “supplier” minimum and “user” maximum.

SnPb - Classification Temperature **Table 6-2**

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
<2.5 mm	240 +0/-5 °C	225 +0/-5 °C
≥ 2.5 mm	225 +0/-5 °C	225 +0/-5 °C

Pb-free - Classification Temperature **Table 6-3**

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6mm	260 ℃	260 ℃	260 ℃
1.6 mm - 2.5mm	260 ℃	250 ℃	245 ℃
> 2.5mm	250 ℃	245 ℃	245 ℃

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7 Storage Condition

7.1 Moisture Sensitivity Level

JL7012A is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-033.

7.2 Storage Alert

1. Calculated shelf life in sealed bag 12 months at＜40°C and 90% relative humidity (RH).
2. Peak package body temperature≤260°C.
3. After bag is opened,devices that will be subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions≤30°C/60%RH or stored per J-STD-033.
4. Devices require bake before mounting if humidity indicator card reads ＞ 10% for level 2a-5a devices or＞60% for level 2 devices when read at 23±5°C,or 3a or 3b are not met.
5. Please refer to IPC/JEDEC J-STD-033 for baking procedure if necessary.

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8 Revision History

Date	Revision	Description
2022.02.09	V1.0	Initial Release;
2022.04.08	V1.1	Modify Pin Assignment (PIN41 update to DACRP); Update DAC Characteristics.
2022.06.08	V1.2	Add IC Marking Information & Solder-Reflow Condition; Add BLE Parameters.
2022.12.01	V1.3	PIN8 Delete GPIO PB8.
2023.03.01	V1.4	Update Features.
2023.10.24	V1.5	Update JL7012A BT_Features.
2023.12.27	V1.6	Update JL7012A BT_Features(Meet class1 transmitting power requirement); Add ESD protection in Section 3.9; Update BLE Characteristics.
2024.08.09	V1.7	Update Audio & PMU_Features; Update IC Marking Information.
2025.01.13	V2.0	Update Bluetooth Vision.
2025.02.28	V2.1	Update Package Information.

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